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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,527	03/24/2006	Kiyoshi Kato	0756-7660	5487

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EXAMINER	
WOLDEGEORGIS, ERMIAS T	

ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,527	KATO ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-9,11-13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-9,11-13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *NPL*

DETAILED ACTION

1. ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 September 2010 has been entered.

2. ***Response to amendment***

Claims 3, 6, 10 and 14 have been cancelled; claims 1, 2, 4-5, 7-9, 11-13 and 15-16 have been amended; claims 17-21 have been newly added; and claims 1, 2, 4-5, 7-9, 11-13 and 15-21 are currently pending.

3. ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

4. ***Claim Rejections - 35 USC § 102/103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4-5, 7-9, 11-13 and 15-16 are rejected under 35 U.S.C. 103(a) as unpatentable over Koyama et al. **(US. 2002/0126108 A1, hereinafter "Koyama")** in view of Eichman et al. **(USPN 5457649, hereinafter "Eichman"),** Young **(USPN 5798534, hereinafter "Young"), and** Yamazaki et al. **(USPN 5854494, hereinafter "Yamazaki").**

In regards to claims 1 and 7, Koyama discloses (Figs. 26(A)-27(B)) a memory device comprising a memory cell **(memory portion, Fig. 27(B))** formed over an insulating surface

(2602), which includes a semiconductor film **(2606)** having two impurity regions **(2636/2637)** a region therebetween, a gate electrode **(2617/2752)** formed over the region with an insulating film **(2608)** interposed therebetween, and two wirings **(2767/2768)** connected to the respective impurity regions **(2636/2637)**, wherein the semiconductor film **(2606)** interposed between the two wirings **(2767/2768)** of the memory cell **(memory portion, Fig. 27(B))** is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings ***(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)***.

In regards to claims 4 and 11, Koyama discloses (Figures 26(A)-27(B)) a memory device comprising a first memory cell and a second memory cell *(though a single memory sell is shown, it is apparent that plurality of memory cells are formed throughout the substrate)* formed over an insulating surface **(2602)**, each of which includes a semiconductor film **(2606)** having two impurity regions **(2636/2637)** and a region therebetween, a gate electrode **(2617/2752)** formed over the region with an insulating film **(2608)** interposed therebetween, and two wirings **(2767/2768)** connected to the respective impurity regions **(2636/2637)**, wherein the first memory cell comprises an initial state ***(inherently there at least one bit to tell whether data is stored or not)***; and the semiconductor film **(2606)** interposed between the two wirings **(2767/2768)** of the second memory cell **(2774)** is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings ***(since the material used***

for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here).

In regards to claim 15, Koyama discloses (Figures 26(A)-27(B)) a manufacturing method of a memory device, comprising the steps of: forming an island shape semiconductor film **(2606)** over an insulating surface **(2602)**; forming a gate insulating film **(2608])** over the island shape semiconductor film **(2606)**; forming a gate electrode **(2617)** over the gate insulating film **(2608)**; doping an N-type impurity element **(Par [0284])** with the gate electrode **(2617)** used as a mask **(Par [0289-0290])**, thereby forming an N-type high concentration impurity region **(2637/2638)** in the island shape semiconductor film **(2606)**; forming an interlayer film **(2761/2762)** over the gate insulating film **(2608)** and the gate electrode **(2617)**; forming a contact hole **(Par [0298])** in the interlayer film **(2761/2762)** and a wiring **(2767/2768)** connected to the high concentration impurity region **(2636/2637)**, thereby forming a memory cell **(memory 2774)**, and applying a voltage between the gate electrode and the wiring of the memory cell, thereby altering a channel region of the island shape semiconductor film to an insulating state ***(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)***.

In regards to claims 1, 4, 7, 11 and 15, Koyama fails to explicitly teach a potential of the gate electrode is changed, and the gate electrode and the semiconductor film are formed in contact with the insulating film.

Eichman while disclosing a write-once (abstract) teaches (Figs. 8, 11 and 12) changing the potential of the external electrode 28 to a breakdown voltage, Vb, to change the state of the a-silicon layer 22.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to change the potential of the gate electrode because as taught by Eichman in col. 10 lines 24-48, this would help write-once irreversibly to the specific memory cell.

However, Koyama as modified by Eichman fails to specifically teach a potential of the gate electrode is changed.

Young while disclosing a method of manufacturing an electronic device (col. 1 lines 6-7) teaches (Fig. 6) a potential of the gate electrode is changed **(col. 7 lines 60-67).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to change gate electrode potential because as taught by Young in col. 7 lines 60-67, having a very high voltage potential would help breaking the link of the specific transistor for the purposed functioning of the semiconductor device.

Yamazaki while disclosing matrix devices including dynamic RAMS (col. 1 lines 16-21) teaches (Figs. 5A-5E) the gate electrode **(65a/65b)** and the semiconductor film **(63a/63b)** are formed in contact with the insulating film **(67)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Koyama by Yamazaki because as taught by Yamazaki in col. 4 lines 47-48, having formed the memory matrix using TFT is simple and provides a sufficient high production yield.

In regards to claims 2, 5, 9, 13 and 16, Yamazaki discloses (Figs. 5A-5E) each memory cell of the memory device comprises two or more gate electrodes **(65a/65b))** on the same insulating film **(64)**.

In regards to claims 3, 6, 10, and 14, Koyama discloses the semiconductor film **(2606)** is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings ***(since the material used for island shape semiconductor layer of the present application and the Koyama reference are the same: a-silicon, it is the property of this material to alter when applying voltage during operation and/or programming of the device. Therefore, a-silicon exhibits the same property as claimed here)***.

In regards to claims 8 and 12, Koyama discloses the electrode **(2617/2752)** is interposed between the two wirings **(2767/2768)**.

6. Claims 17-21 are rejected under 35 U.S.C. 103(a) as unpatentable over Koyama in view of Eichman, Young **and** Yamazaki as applied to claims 1, 4, 7, 11 and 15, and further in view of Zhao et al. **(IEEE ISBN 0-7803-1450-6, hereinafter "Zhao")**

In regards to claims 17-21, Koyama as modified above fails to explicitly teach sidewalls formed on side surfaces of the gate electrode.

Zhao while disclosing TFT device utilizing a polysilicon floating gate spacer (abstract) teaches (Fig. 1) sidewalls **(N+ floating gate poly spacer)** formed on side surfaces of the gate electrode **(N+ poly)**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a polysilicon floating gate spacer on side surfaces of the gate electrode because as taught by Zhao in Page 15.4.1 and 15.4.2 (Abstract/Conclusion), it effectively reduces the OFF state leakage current and suppress the kin effect while maintaining a reasonable ON current.

7. ***Response to Arguments***

Applicant's arguments with respect to claims 1, 4, 7, 11 and 15 have been considered but are moot in view of the new ground(s) of rejection.

8. ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daveinne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893

/A. Sefer/
Primary Examiner
Art Unit 2893